ABSTRACT OF THE INVENTION

ADAPTIVE THREAD ID CACHE MECHANISM FOR AUTONOMIC PERFORMANCE TUNING

An apparatus and method for inhibiting data cache thrashing in a multi-threading execution mode through simulating a higher level of associativity in a data cache. The apparatus temporarily splits a data cache into multiple regions and each region is selected according to a thread ID indicator in an instruction register. The data cache is split when the apparatus is in the multi-threading execution mode indicated by an enable cache split bit.